

FORM PTO-1449

Docket Number (Optional)

Application Number

162.7107USU

09/896,059

Applicant

Bhattacharya et al.

Filing Date

June 29, 2001

Group Art Unit

2825

INFORMATION DISCLOSURE CITATION  
IN AN APPLICATION

(Use several sheets if necessary)

## U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

## OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)

J. P. Fishburn and A. E. Dunlop, AT&T Bell Laboratories, "**TILOS: A Posynomial Programming Approach to Transistor Sizing**", p. 326-328, IEEE, 1985.

George et al., "**Power Analysis and Characterization for Semi-Custom Design**", p. 215-218, IWLPD' 94 Workshop Proceedings.

Ken Scott and Kurt Keutzer, "**Improving Cell Libraries for Synthesis**", IEEE 1994 Custom Integrated Circuits Conference.

Kanwar Jit Singh, "**Performance Optimization of Digital Circuits**", B. Tech (Indian Institute of Technology, Kanpur) 1986 and University of California at Berkeley 1992.

EXAMINER

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13-MARCH-2003

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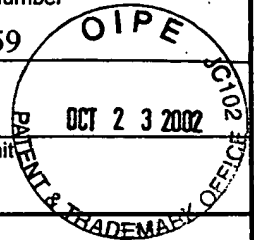
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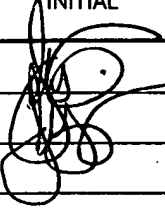
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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,796,128	8/18/98	Tran et al.	257	202	
	6,184,718	2/6/01	Tran et al.	326	121	

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						YES	NO

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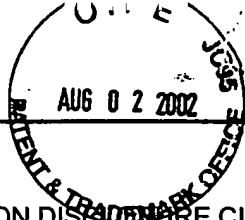

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Randal Bryant, "Symbolic Boolean Manipulation with Ordered Binary-Decision Diagrams", ACM Computing Surveys, vol. 24, No. 3, pp. 293-318 (pp. 1-52), September 1992.

D.G. Chinnery and K. Keutzer, "Closing the Gap Between ASIC and Custom: An ASIC Perspective", University of California at Berkley, 2000.

Olivier Coudert, Ramsey Haddad and Srilatha Manne, "New Algorithms for Gate Sizing: A Comparative Study", Design Automation conference, 1996.

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